AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

In the Claims:

Claims 1-13 (Canceled without prejudice or disclaimer).

14. (Previously Presented) A multilayer wiring board having through holes in a thickness-wise direction,

wherein a semiconductor substrate mounted and superimposed on the multilayer wiring board has through holes formed in a thicknesswise direction thererof, the through holes of the semiconductor substrate being located directly above the through holes of the multilayer wiring board which form thermal vias in the multilayer wiring board, and having areas projected onto the multilayer wiring board, perpendicular thereto, which fall within the through holes of the multilayer wiring board.

15. (Previously Presented) A multilayer wiring board having through holes in a thickness-wise direction which form thermal vias in the multilayer wiring board,

wherein a semiconductor substrate mounted and superimposed on the multilayer wiring board has through holes formed in a thicknesswise direction thereof, the through holes of the semiconductor substrate being located respectively directly above the through-holes of the multilayer wiring board, and having areas projected onto the

multilayer wiring board, perpendicular thereto, which partly overlap the through holes of the multilayer wiring board.

Claim 16. (Canceled).

17. (Previously Presented) A multilayer wiring board having through holes in a thickness-wise direction which form thermal vias in the multilayer wiring board,

wherein a semiconductor substrate mounted on the multilayer wiring board has cross-plane through holes, and heat flows one-dimensionally through the through holes in the semiconductor substrate and the cross-plane through holes in the multilayer wiring board when heat flows out to a surface of the multilayer wiring board opposite to that surface thereof, on which the semiconductor substrate is mounted, via the through holes in the semiconductor substrate and the through holes in the multilayer wiring board by virtue of the through holes in the semiconductor substrate being located relative to the through holes in the multilayer wiring board so that the through holes in the semiconductor substrate have areas projected onto the multilayer wiring board, perpendicular thereto, which fall within the through holes of the multilayer wiring board.

18. (Currently Amended) The multilayer wiring board according to claim 14 or 15, wherein conductive layers are formed on side surfaces of said through holes in said multilayer wiring board~~substrate~~, or interiors of the through holes in said multilayer wiring board ~~substrate~~ and comprise a conductive material.

19. (Currently Amended) The multilayer wiring board according to claim 14 or 15, wherein a semiconductor element is mounted, in which conductive layers are formed on side surfaces of said through holes in said multilayer wiring board~~substrate~~, or interiors of the through holes in said multilayer wiring board ~~substrate~~ and comprise a conductive material.

20. (Previously Presented) The multilayer wiring board according to claim 14, wherein wirings, which connect heating areas in the semiconductor substrate mounted on the multilayer wiring board, are electrically connected to the through holes in the semiconductor substrate, and electrical connection is effected through the heating areas, the wirings, the through holes of the semiconductor substrate, the through holes of the multilayer wiring board, and a surface of the multilayer wiring board, on which the semiconductor substrate is not mounted, in this order.

21. (Previously Presented) A multilayer wiring board having cross-plane through holes in said multilayer wiring board which form thermal vias in the multilayer wiring board, wherein said through holes extend in a direction substantially orthogonal to a planar direction of a major surface of the multilayer wiring board,

wherein said through holes are distributed in the multilayer wiring board to be aligned relative to at least one transistor of a semiconductor substrate mounted on the multilayer wiring board such that a distribution of heat dissipated from the transistor in said planar direction is substantially identical with a distribution of the through holes in said planar direction.

22. (Previously Presented) A multilayer wiring board having cross-plane through holes in said multilayer wiring board which form thermal vias in the multilayer wiring board, wherein said through holes extend in a direction substantially orthogonal to a planar direction of a major surface of the multilayer wiring board,

wherein said through holes are distributed in the multilayer wiring board to be aligned relative to at least one transistor of a semiconductor substrate mounted on the multilayer wiring board such that a distribution of heat dissipated from the transistor in said planar direction is substantially identical with a distribution of large and small cross-section areas of the through holes in said planar direction.

23. (Previously Presented) A multilayer wiring board,

wherein a semiconductor substrate having cross-plane through holes, which are connected to emitter wirings connected to emitters of heterojunction bipolar transistors and extended through the semiconductor substrate and which have conductive layers on sides thereof or inside thereof, is mounted on the multilayer wiring board, and the cross-plane through holes in the semiconductor substrate and through holes extending through the multilayer wiring board which form thermal vias in the multilayer wiring board are connected to each other, and wherein conductive layers are provided on sides of or inside of the connected through holes in the semiconductor substrate and the multilayer wiring board, and the through holes in the semiconductor substrate have areas projected onto the multilayer wiring board, perpendicular thereto, which fall within the through holes in the multilayer wiring board.

Claim 24. (Canceled).

25. (Previously Presented) A semiconductor device including a plurality of finger-shaped emitter electrodes or source electrodes, and at least one via hole which are arranged in rows in a first direction on a semiconductor substrate,

wherein the emitter electrodes or the source electrodes are connected to a conductive layer formed on a back surface opposite to a surface, on which the electrodes are formed, through the via hole, and

wherein said rows comprising the emitter electrodes or source electrodes, and the via holes are arranged in parallel in a second direction orthogonal to the first direction, and the via holes are positionally shifted from one another in adjacent rows among said rows, or adjacent rows are positionally shifted from one another in the first direction, wherein a multilayer wiring board has through holes which form thermal vias in the multilayer wiring board formed on sides thereof or inside thereof with a conductive layer, and areas, which the via holes of the semiconductor device occupies, overlap areas which the through holes of the multilayer wiring board occupy in a plane orthogonal to a thickness-wise direction of the multilayer wiring board.

26. (Currently Amended) A multilayer wiring board,

wherein emitter electrodes of heterojunction bipolar transistors are arranged on a semiconductor substrate including through holes, the semiconductor substrate is mounted on a wiring board, which wiring board has cross-plane through holes which form thermal vias in the wiring board, and said through holes in the wiring board have

on sides or inside thereof a material of good thermal conductivity, wherein the emitter electrodes are disposed in a group electrically connected by a common emitter wiring located in a plane over the semiconductor substrate, wherein emitter electrodes in a central area of the group are located over areas which the through holes in the wiring board occupy, and wherein first and second end emitter electrodes are respectively disposed at opposite ends of the emitter electrodes in the central area of the group to protrude from the areas which the through holes in the wiring board occupy, the through holes of the semiconductor substrate being located directly above the through holes in said multilayer wiring boardsubstrate, and having areas projected onto the multilayer wiring board, perpendicular thereto, which fall within the through holes of the multilayer wiring board.

27. (Currently Amended) A multilayer wiring board having through holes which form thermal vias in the multilayer wiring board, wherein emitter electrodes of heterojunction bipolar transistors are arranged in line on a semiconductor substrate, said semiconductor substrate is mounted on said multilayer wiring board, and said multilayer wiring board has cross-plane through holes, said through holes in the multilayer wiring board having formed on sides or inside thereof a conductive material, of higher different than a material comprising the multilayer wiring board, said conductive material having a higher thermal conductivity than that a thermal conductivity of the material comprising the of the multilayer wiring board,

wherein said emitter electrodes are arranged in a line to form groups, such that all emitter electrodes in a group are connected with a common emitter wiring, wherein

each group includes central emitter electrodes located between first and second end emitter electrodes, wherein said first and second end emitter electrodes are located, respectively, at opposite ends of the central emitter electrodes, and

wherein, with respect to a positional relation viewed from a normal direction to an in-plane surface of said multilayer wiring board, the central emitter electrodes in each of said groups of said emitter electrodes are included in an area which said through holes in said multilayer wiring ~~substrate~~ board occupy, but the first and second end emitter electrodes of each of said groups of said emitter electrodes protrude from the area which said through holes in said multilayer wiring ~~substrate~~ board occupy.

28. (Previously Presented) A multilayer wiring board according to claim 14, wherein said semiconductor substrate includes emitter electrodes located on a first main surface of the semiconductor substrate and a plated heat sink located on a second main surface of the semiconductor substrate, opposite to said first main surface, wherein the plated heat sink is connected to the multilayer wiring board.

29. (Previously Presented) A multilayer wiring board according to claim 28, wherein the through holes in the semiconductor substrate extend between the first and second main surfaces of the semiconductor substrate.

30. (Previously Presented) A multilayer wiring board according to claim 29, wherein said plated heat sink is connected to the multilayer wiring board by a brazing layer.

31. (Previously Presented) A multilayer wiring board according to claim 15, wherein the through holes in the semiconductor substrate extend between first and second main surfaces of the semiconductor substrate.

32. (Previously Presented) A multilayer wiring board according to claim 14, wherein the through holes in the semiconductor substrate extend between first and second main surfaces of the semiconductor substrate.

33. (Previously Presented) A multilayer wiring board according to claim 32, wherein a plated heat sink is connected to the multilayer wiring board by a brazing layer.

Claims 34 and 35. (Canceled).

36. (Previously Presented) A multilayer wiring board according to claim 17, wherein said semiconductor substrate includes emitter electrodes located on a first main surface of the semiconductor substrate and a plated heat sink located on a second main surface of the semiconductor substrate, opposite to said first main surface, wherein the plated heat sink is connected to the multilayer wiring board.

37. (Previously Presented) A multilayer wiring board according to claim 36, wherein the through holes in the semiconductor substrate extend between the first and second main surfaces of the semiconductor substrate.

38. (Previously Presented) A multilayer wiring board according to claim 37, wherein said plated heat sink is connected to the multilayer wiring board by a brazing layer.

39. (Previously Presented) A multilayer wiring board according to claim 21, wherein said semiconductor substrate includes emitter electrodes located on a first main surface of the semiconductor substrate and a plated heat sink located on a second main surface of the semiconductor substrate, opposite to said first main surface, wherein the plated heat sink is connected to the multilayer wiring board.

40. (Previously Presented) A multilayer wiring board according to claim 39, wherein said plated heat sink is connected to the multilayer wiring board by a brazing layer.

41. (Previously Presented) A multilayer wiring board according to claim 22, wherein said semiconductor substrate includes emitter electrodes located on a first main surface of the semiconductor substrate and a plated heat sink located on a second main surface of the semiconductor substrate, opposite to said first main surface, wherein the plated heat sink is connected to the multilayer wiring board.

42. (Previously Presented) A multilayer wiring board according to claim 41, wherein the through holes in the semiconductor substrate extend between the first and second main surfaces of the semiconductor substrate.

43. (Previously Presented) A multilayer wiring board according to claim 23, wherein said semiconductor substrate includes emitter electrodes located on a first main surface of the semiconductor substrate and a plated heat sink located on a second main surface of the semiconductor substrate, opposite to said first main surface, wherein the plated heat sink is connected to the multilayer wiring board.

44. (Previously Presented) A multilayer wiring board according to claim 43, wherein the through holes in the semiconductor substrate extend between the first and second main surfaces of the semiconductor substrate.

45. (Previously Presented) A multilayer wiring board according to claim 44, wherein said plated heat sink is connected to the multilayer wiring board by a brazing layer.

46. (Previously Presented) A multilayer wiring board according to claim 25, wherein said semiconductor substrate includes emitter electrodes located on a first main surface of the semiconductor substrate and a plated heat sink located on a second main surface of the semiconductor substrate, opposite to said first main surface, wherein the plated heat sink is connected to the multilayer wiring board.

47. (Previously Presented) A multilayer wiring board according to claim 46, wherein said plated heat sink is connected to the multilayer wiring board by a brazing layer.

48. (Previously Presented) A multilayer wiring board according to claim 26, wherein said semiconductor substrate includes emitter electrodes located on a first main surface of the semiconductor substrate and a plated heat sink located on a second main surface of the semiconductor substrate, opposite to said first main surface, wherein the plated heat sink is connected to the multilayer wiring board.

49. (Previously Presented) A multilayer wiring board according to claim 48, wherein said plated heat sink is connected to the multilayer wiring board by a brazing layer.

50. (Previously Presented) The multilayer wiring board according to claim 14, wherein said thicknesswise direction is a direction of a Z-axis of the multilayer wiring board, and wherein an entirety of each of the projected areas in an XY plane, perpendicular to the Z axis, falls within an area in the XY plane of a corresponding through hole of the multilayer wiring board.

Claim 51. (Canceled).

52. (Previously Presented) The multilayer wiring board according to claim 17, wherein said thicknesswise direction is a direction of a Z-axis of the multilayer wiring board, and wherein an entirety of each of the projected areas in an XY plane, perpendicular to the Z-axis, falls within an area in the XY plane of a corresponding through hole of the multilayer wiring board.

53. (Previously Presented) The multilayer wiring board according to claim 23, wherein said thicknesswise direction is a direction of a Z-axis of the multilayer wiring board, and wherein an entirety of each of the projected areas in an XY plane, perpendicular to the Z-axis, falls within an area in the XY plane of a corresponding through hole of the multilayer wiring board.

54. (Previously Presented) The multilayer wiring board according to claim 26, wherein said thicknesswise direction is a direction of a Z-axis of the multilayer wiring board, and wherein an entirety of each of the projected areas in an XY plane, perpendicular to the Z-axis, falls within an area in the XY plane of a corresponding through hole of the multilayer wiring board.